• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Features

■Low $R_{DS(ON)}$ to minimize conductive loss

■Low Gate Charge for fast switching

■Low Thermal resistance

■AEC-Q101 Qualified

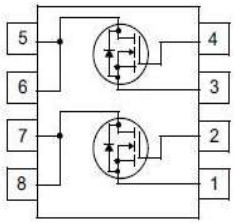
•Application

■BLDC Motor driver

■DC-DC

■Battery protection

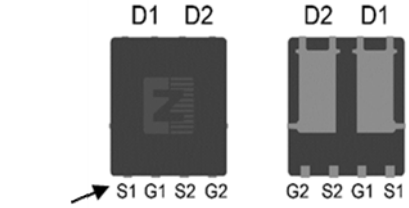
• Product Summary



V_{DS}= 60V

$R_{DS(ON)}$ = 7.6mΩ

I_D= 52A



DFN5*6

•Ordering Information:

Part NO.	ZMDA68608N
Marking	ZMD68608
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

•Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	52	A
	I_D	T_C=75℃	42	A
	I_D	T_C=100℃	37	A
Pulsed Drain Current ①	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	208	A
Total Power Dissipation	P_D	T_C=25℃	52	W
Total Power Dissipation	P_D	T_A=25℃	3.0	W
Operating Junction Temperature	T_J		-55 to +175	℃
Storage Temperature	T_{STG}		-55 to +175	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, VGS=10V, Rg=25Ω,	12	mJ
		L=0.5mH, VGS=10V, Rg=25Ω,	21	mJ
ESD Level (HBM)			CLASS 2	

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	2.9	°C/W
Thermal resistance, junction-ambient	$R_{thJA①}$		-	50	°C/W
Soldering temperature（total time<10s)	Tsold		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	2	2.6	4	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= 60V	-	-	1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V	-	-	100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D= 14A	-	7.6	9.5	mΩ
Forward Transconductance	g_{FS}	V_{GS} =5V, I_{SD} = 5A	-	14	-	S
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = 14A	-	-	1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=25V	-	1196	-	pF
Output capacitance	Coss		-	661	-	
Reverse transfer capacitance	Crss		-	47	-	
Gate Risistance	Rg	f = 1MHz	-	1.2	-	Ω
Total gate charge	Qg	V_{DD} = 30V, I_D = 14A, V_{GS} = 10V	-	19	-	nC
Gate - Source charge	Qgs		-	4.9	-	
Gate - Drain charge	Qgd		-	5.5	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V, R_G =3.3Ω, I_D =20A	-	6	-	ns
Turn-ON Rise time	t_r		-	4	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	11	-	ns
Turn-Off Fall time	t_f		-	7	-	ns
Reverse Recovery Time	t_{rr}	V_{DD}=20V, dI_S/dt = 100A/us, I_S=20A	-	26	-	ns
Reverse Recovery Charge	Q_{rr}		-	16	-	nC

Fig.1 Gate-Charge Characteristics

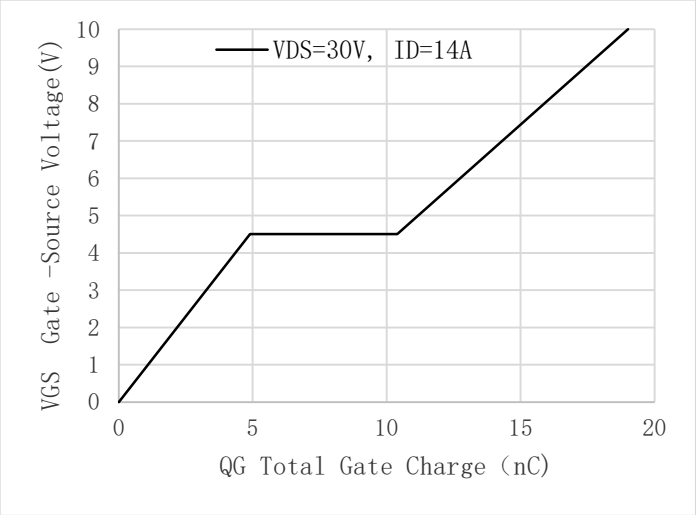


Fig.2 Capacitance Characteristics

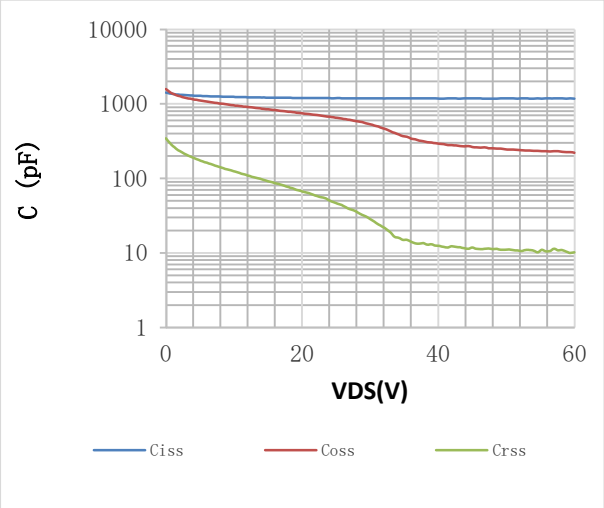


Fig.3 Power Dissipation

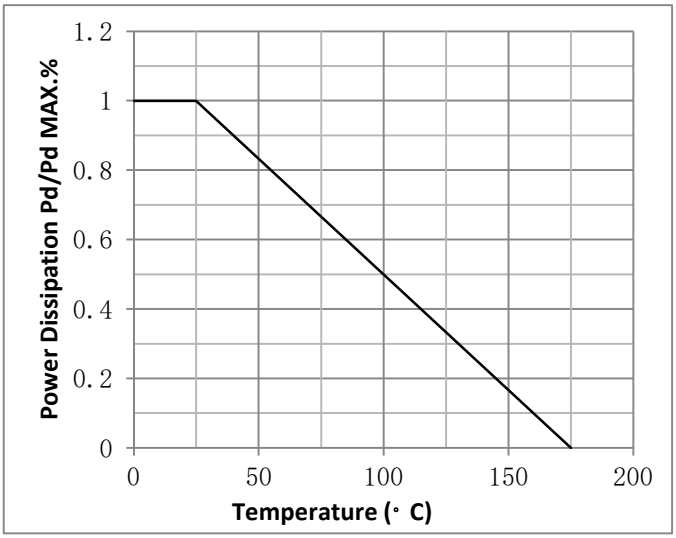


Fig.4 Typical output Characteristics

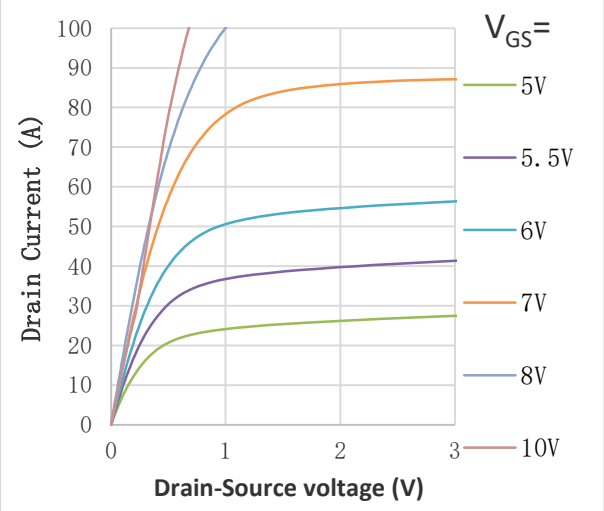


Fig.5 Threshold Voltage V.S Junction Temperature

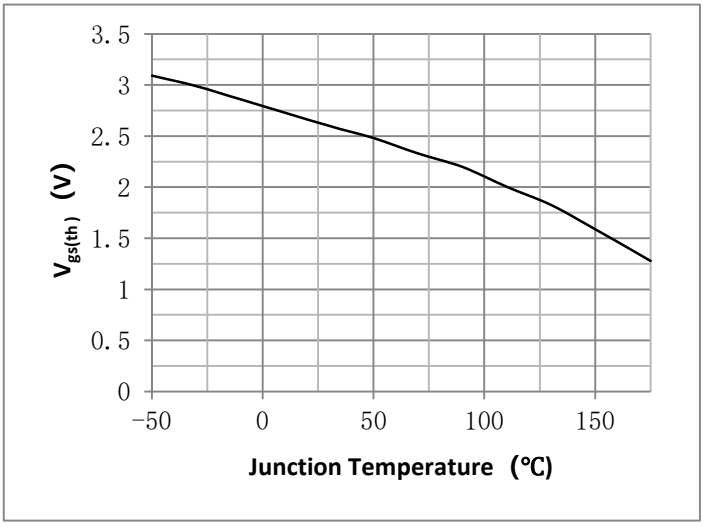


Fig.6 Resistance V.S Drain Current

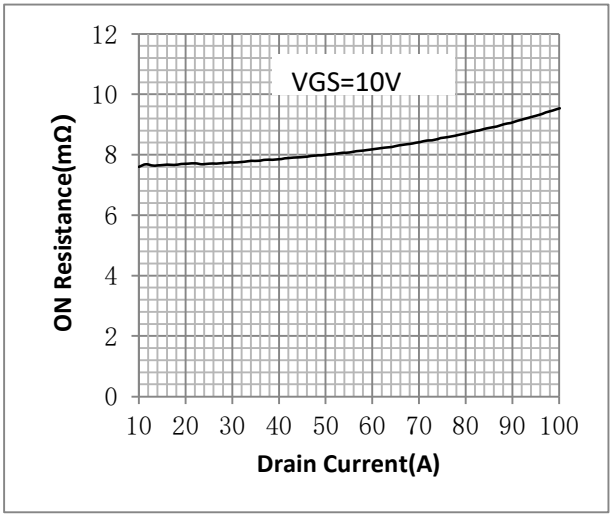


Fig.7 On-Resistance VS Gate Source Voltage

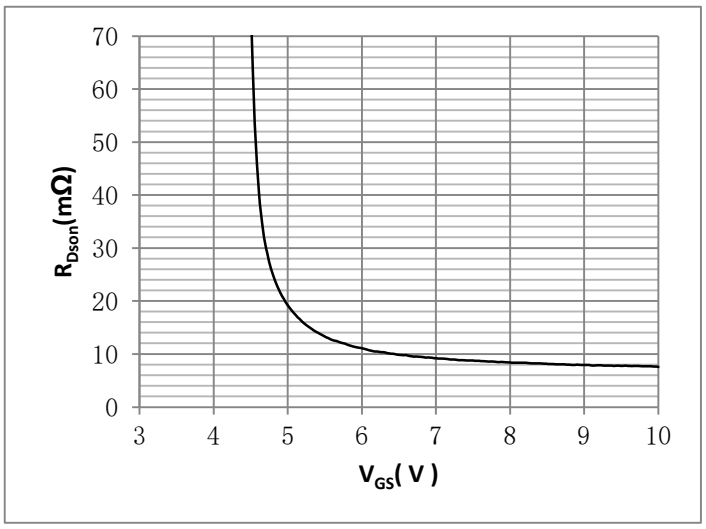


Fig.8 On-Resistance V.S Junction Temperature

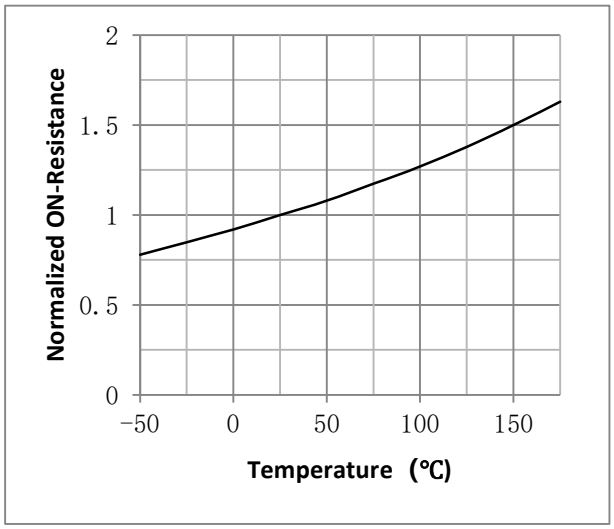


Figure 9. Diode Forward Voltage vs. Current

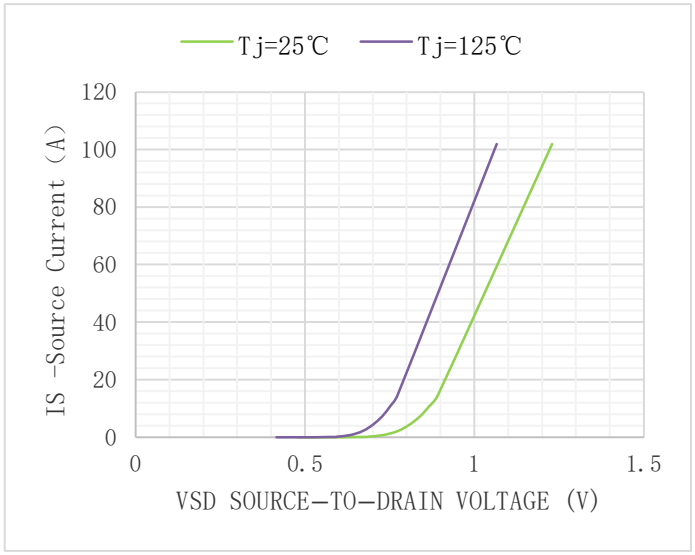


Figure 10. Transfer Characteristics

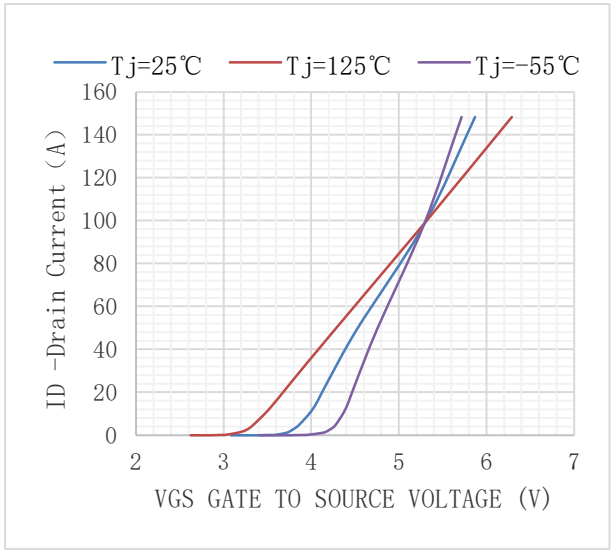


Fig.11 SOA Maximum Safe Operating Area

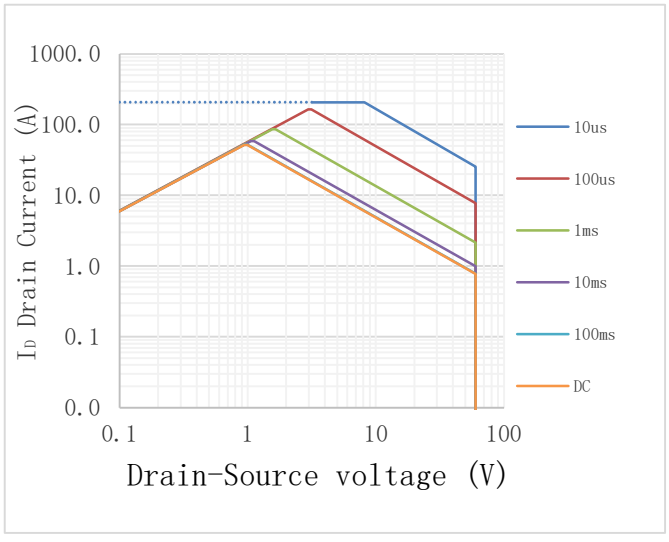
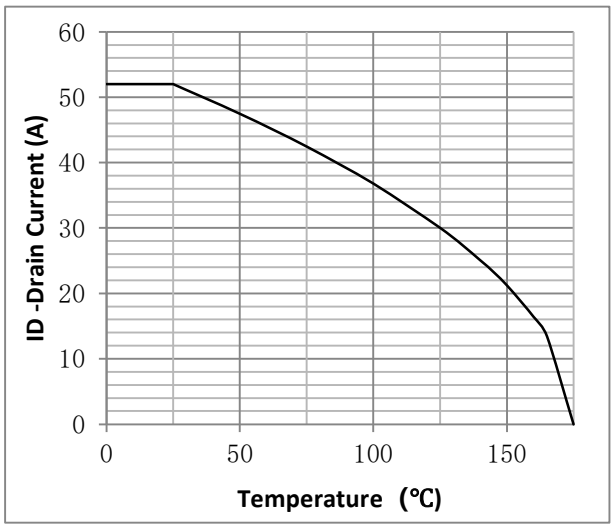
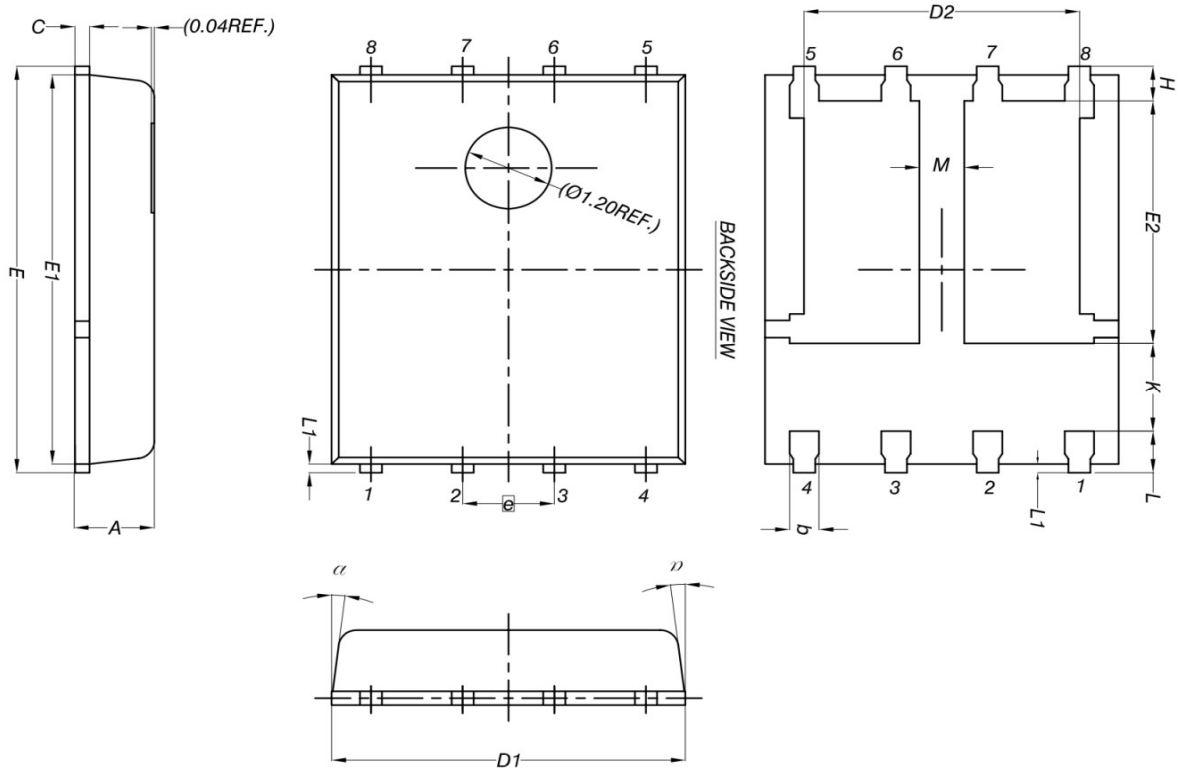


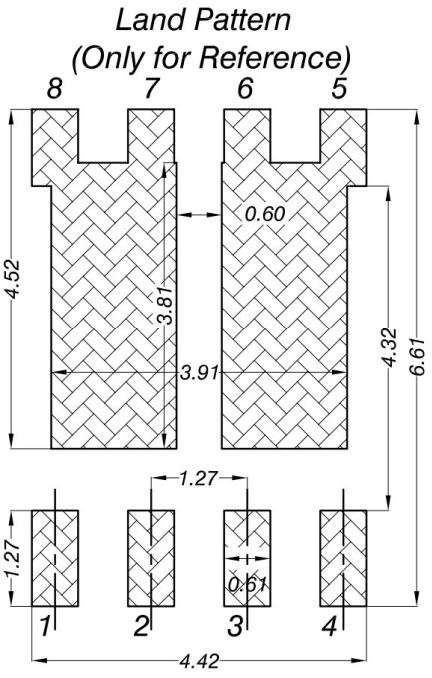
Fig.12 ID vs. Case Temperature③



●DFN5*6 Package Outline



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°



Note:

① Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=+20V/-10V, Tj=175℃, t=1000 hours；

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

③Practically the current will be limited by PCB, thermal design and operating temperature. VGS=10V.

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Revision History

Version	Date	Change
A	2024.12.19	New